

| | L # | Hits | Search Text | DBs |
|---|-----|-------|--|--------------------|
| 1 | L1 | 59740 | (bit field tag flag cod\$3 encod\$3) near10 instruction | USPAT; US-PGPUB |
| 2 | L12 | 24001 | (register argument variable static parameter value) near10 (sav\$3 stor\$3) near20 ((stack frame region space area pointer locat\$3 position) near10 (call\$3 different separate\$3 first second subroutine above below minus plus subtract\$3 add\$3)) | USPAT; US-PGPUB |
| 3 | L13 | 399 | 1 near99 12 | USPAT; US-PGPUB |
| 4 | L14 | 11017 | (register argument variable static parameter value) near10 (sav\$3 stor\$3) near20 ((stack frame region space area pointer) near10 (call\$3 different separate\$3 second subroutine above below minus plus subtract\$3 add\$3)) | USPAT; US-PGPUB |
| 5 | L16 | 235 | 13 not 15 | USPAT; US-PGPUB |
| 6 | L15 | 164 | 1 near99 14 | USPAT; US-PGPUB |

| | Document ID | U | Title | Current OR |
|----|------------------------------|-------------------------------------|--|------------|
| 1 | US 20040 02515 0 A1 | <input type="checkbox"/> | Compiler, compiler apparatus and compilation method | 717/154 |
| 2 | US 20030 18813 7 A1 | <input checked="" type="checkbox"/> | Parallel subword instructions with distributed results | 712/221 |
| 3 | US 20030 15435 8 A1 | <input checked="" type="checkbox"/> | Apparatus and method for dispatching very long instruction word having variable length | 712/24 |
| 4 | US 20030 13584 8 A1 | <input checked="" type="checkbox"/> | Use of multiple procedure entry and/or exit points to improve instruction scheduling | 717/158 |
| 5 | US 20030 12641 0 A1 | <input checked="" type="checkbox"/> | System and method of reducing the number of copies from alias registers to real registers in the commitment of instructions | 712/218 |
| 6 | US 20030 11557 9 A1 | <input checked="" type="checkbox"/> | Optimizing source code for iterative execution | 717/152 |
| 7 | US 20030 06149 9 A1 | <input checked="" type="checkbox"/> | Data encryption and decryption | 713/189 |
| 8 | US 20030 03350 4 A1 | <input checked="" type="checkbox"/> | Micro-controller for reading out compressed instruction code and program memory for compressing instruction code and storing therein | 712/210 |
| 9 | US 20030 03348 2 A1 | <input checked="" type="checkbox"/> | Micro-controller for reading out compressed instruction code and program memory for compressing instruction code and storing therein | 711/119 |
| 10 | US 20030 02383 7 A1 | <input checked="" type="checkbox"/> | Register file backup queue | 712/228 |
| 11 | US 20030 00526 8 A1 | <input checked="" type="checkbox"/> | Find first bit value instruction | 712/223 |
| 12 | US 20020 19667 8 A1 | <input checked="" type="checkbox"/> | Eliminating store/restores within hot function prolog/epilogs using volatile registers | 365/200 |
| 13 | US 20020 16996 9 A1 | <input checked="" type="checkbox"/> | Information processing unit having tamper - resistant system | 713/190 |
| 14 | US 20020 14790 1 A1 | <input checked="" type="checkbox"/> | Method of handling instructions within a processor with decoupled architecture, in particular a processor for digital signal processing, and corresponding processor | 712/225 |
| 15 | US 20020 14408 4 A1 | <input checked="" type="checkbox"/> | Processor for executing highly efficient VLIW | 712/24 |
| 16 | US 20020 13871 5 A1 | <input checked="" type="checkbox"/> | Microprocessor executing data transfer between memory and register and data transfer between registers in response to single push/pop instruction | 712/225 |
| 17 | US 20020 12922 3 A1 | <input checked="" type="checkbox"/> | Processor for executing highly efficient VLIW | 712/24 |

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| 18 | US 20020 12416 0 A1 | <input checked="" type="checkbox"/> | Register file backup queue | 712/228 |
| 19 | US 20020 12404 4 A1 | <input checked="" type="checkbox"/> | Method of handling branching instructions within a processor, in particular a processor for digital signal processing, and corresponding processor | 709/200 |
| 20 | US 20020 08785 1 A1 | <input checked="" type="checkbox"/> | Microprocessor and an instruction converter | 712/239 |
| 21 | US 20020 06247 9 A1 | <input checked="" type="checkbox"/> | Microcontroller with modifiable program | 717/168 |
| 22 | US 20020 04290 9 A1 | <input checked="" type="checkbox"/> | Retargetable compiling system and method | 717/149 |
| 23 | US 20020 03286 8 A1 | <input checked="" type="checkbox"/> | Information processing apparatus, executable module generating method, and storage medium | 713/193 |
| 24 | US 20020 03271 8 A1 | <input checked="" type="checkbox"/> | METHOD AND APPARATUS FOR MAINTAINING TRANSLATED ROUTINE STACK IN A BINARY TRANSLATION ENVIROMENT | 718/107 |
| 25 | US 20020 01990 2 A1 | <input checked="" type="checkbox"/> | Stack switching mechanism in a computer system | 710/260 |
| 26 | US 20020 01389 3 A1 | <input checked="" type="checkbox"/> | Real time debugger interface for embedded systems | 712/227 |
| 27 | US 20020 01085 1 A1 | <input checked="" type="checkbox"/> | Emulated branch effected by trampoline mechanism | 712/244 |
| 28 | US 20020 00745 0 A1 | <input checked="" type="checkbox"/> | Line-oriented reorder buffer | 712/23 |
| 29 | US 66979 36 B2 | <input checked="" type="checkbox"/> | Register file backup queue | 712/228 |
| 30 | US 66878 57 B1 | <input checked="" type="checkbox"/> | Microcomputer which can execute a monitor program supplied from a debugging tool | 714/38 |
| 31 | US 66548 78 B1 | <input checked="" type="checkbox"/> | Register bit scanning | 712/234 |
| 32 | US 66314 60 B1 | <input checked="" type="checkbox"/> | Advanced load address table entry invalidation based on register address wraparound | 712/217 |
| 33 | US 65913 85 B1 | <input checked="" type="checkbox"/> | Method and apparatus for inserting programmable latency between address and data information in a memory tester | 714/718 |
| 34 | US 65359 03 B2 | <input checked="" type="checkbox"/> | Method and apparatus for maintaining translated routine stack in a binary translation environment | 718/100 |
| 35 | US 65127 75 B1 | <input checked="" type="checkbox"/> | Method and apparatus for a programmable bitstream parser for audiovisual and generic decoding systems | 370/428 |
| 36 | US 65052 96 B2 | <input checked="" type="checkbox"/> | Emulated branch effected by trampoline mechanism | 712/244 |

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| 37 | US 65022 37 B1 | <input checked="" type="checkbox"/> | Method and apparatus for performing binary translation method and apparatus for performing binary translation | 717/136 |
| 38 | US 64991 00 B1 | <input checked="" type="checkbox"/> | Enhanced instruction decoding | 712/210 |
| 39 | US 64899 63 B2 | <input checked="" type="checkbox"/> | Application program interface for a graphics system | 345/522 |
| 40 | US 64571 71 B1 | <input checked="" type="checkbox"/> | Storage structure for dynamic management of translated code blocks in dynamic object code translation | 717/138 |
| 41 | US 64497 36 B1 | <input checked="" type="checkbox"/> | Method and apparatus for providing chained breakpoints in a microprocessor | 714/35 |
| 42 | US 64461 97 B1 | <input checked="" type="checkbox"/> | Two modes for executing branch instructions of different lengths and use of branch control instruction and register set loaded with target instructions | 712/237 |
| 43 | US 64426 73 B1 | <input checked="" type="checkbox"/> | Update forwarding cache for address mode | 712/202 |
| 44 | US 64083 80 B1 | <input checked="" type="checkbox"/> | Execution of an instruction to load two independently selected registers in a single cycle | 712/225 |
| 45 | US 64083 75 B2 | <input checked="" type="checkbox"/> | System and method for register renaming | 712/23 |
| 46 | US 63973 19 B1 | <input checked="" type="checkbox"/> | Process for executing highly efficient VLIW | 712/24 |
| 47 | US 63972 35 B1 | <input checked="" type="checkbox"/> | Data processing device and method of computing the costine transform of a matrix | 708/401 |
| 48 | US 63816 89 B2 | <input checked="" type="checkbox"/> | Line-oriented reorder buffer configured to selectively store a memory operation result in one of the plurality of reorder buffer storage locations corresponding to the executed instruction | 712/215 |
| 49 | US 63743 47 B1 | <input checked="" type="checkbox"/> | Register file backup queue | 712/228 |
| 50 | US 63603 09 B1 | <input checked="" type="checkbox"/> | System and method for assigning tags to control instruction processing in a superscalar processor | 712/23 |
| 51 | US 63213 31 B1 | <input checked="" type="checkbox"/> | Real time debugger interface for embedded systems | 712/244 |
| 52 | US 62826 33 B1 | <input checked="" type="checkbox"/> | High data density RISC processor | 712/208 |
| 53 | US 62726 17 B1 | <input checked="" type="checkbox"/> | System and method for register renaming | 712/23 |
| 54 | US 62601 90 B1 | <input checked="" type="checkbox"/> | Unified compiler framework for control and data speculation with recovery code | 717/156 |
| 55 | US 62508 21 B1 | <input checked="" type="checkbox"/> | Method and apparatus for processing branch instructions in an instruction buffer | 712/238 |
| 56 | US 62498 62 B1 | <input checked="" type="checkbox"/> | Dependency table for reducing dependency checking hardware | 712/218 |
| 57 | US 62471 20 B1 | <input checked="" type="checkbox"/> | Instruction buffer for issuing instruction sets to an instruction decoder | 712/238 |
| 58 | US 62405 44 B1 | <input checked="" type="checkbox"/> | Simulation system, simulation evaluation system, simulation method, and computer-readable memory containing a simulation program, having less trace information for reverse execution | 717/135 |

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|----|----------------------|-------------------------------------|---|---------------|
| 59 | US 62370 82 B1 | <input checked="" type="checkbox"/> | Reorder buffer configured to allocate storage for instruction results corresponding to predefined maximum number of concurrently receivable instructions independent of a number of instructions received | 712/215 |
| 60 | US 62267 89 B1 | <input checked="" type="checkbox"/> | Method and apparatus for data flow analysis | 717/138 |
| 61 | US 62197 79 B1 | <input checked="" type="checkbox"/> | Constant reconstructing processor which supports reductions in code size | 712/210 |
| 62 | US 62090 84 B1 | <input checked="" type="checkbox"/> | Dependency table for reducing dependency checking hardware | 712/233 |
| 63 | US 61990 95 B1 | <input checked="" type="checkbox"/> | System and method for achieving object method transparency in a multi-code execution environment | 718/107 |
| 64 | US 61957 40 B1 | <input checked="" type="checkbox"/> | Constant reconstructing processor that execute an instruction using an operand divided between instructions | 712/24 |
| 65 | US 61382 31 A | <input checked="" type="checkbox"/> | System and method for register renaming | 712/216 |
| 66 | US 61346 51 A | <input checked="" type="checkbox"/> | Reorder buffer employed in a microprocessor to store instruction results having a plurality of entries predetermined to correspond to a plurality of functional units | 712/215 |
| 67 | US 61287 22 A | <input checked="" type="checkbox"/> | Data processing system having an apparatus for exception tracking during out-of-order operation and method therefor | 712/23 |
| 68 | US 61254 56 A | <input checked="" type="checkbox"/> | Microcomputer with self-diagnostic unit | 714/25 |
| 69 | US 61087 69 A | <input checked="" type="checkbox"/> | Dependency table for reducing dependency checking hardware | 712/216 |
| 70 | US 60918 97 A | <input checked="" type="checkbox"/> | Fast translation and execution of a computer program on a non-native architecture by use of background translator | 717/138 |
| 71 | US 60853 06 A | <input checked="" type="checkbox"/> | Processor for executing highly efficient VLIW | 712/24 |
| 72 | US 60617 85 A | <input checked="" type="checkbox"/> | Data processing system having an apparatus for out-of-order register operations and method therefor | 712/236 |
| 73 | US 60264 82 A | <input checked="" type="checkbox"/> | Recorder buffer and a method for allocating a fixed amount of storage for instruction results independent of a number of concurrently dispatched instructions | 712/215 |
| 74 | US 60095 08 A | <input checked="" type="checkbox"/> | System and method for addressing plurality of data values with a single address in a multi-value store on FIFO basis | 712/41 |
| 75 | US 60000 28 A | <input checked="" type="checkbox"/> | Means and apparatus for maintaining condition codes in an unevaluated state | 712/226 |
| 76 | US 59960 58 A | <input checked="" type="checkbox"/> | System and method for handling software interrupts with argument passing | 712/31 |
| 77 | US 59872 35 A | <input checked="" type="checkbox"/> | Method and apparatus for predecoding variable byte length instructions for fast scanning of instructions | 712/210 |
| 78 | US 59616 34 A | <input checked="" type="checkbox"/> | Reorder buffer having a future file for storing speculative instruction execution results | 712/218 |
| 79 | US 59516 76 A | <input checked="" type="checkbox"/> | Apparatus and method for direct loading of offset register during pointer load operation | 712/225 |
| 80 | US 59464 68 A | <input checked="" type="checkbox"/> | Reorder buffer having an improved future file for storing speculative instruction execution results | 712/218 |

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|-----|---------------------|-------------------------------------|--|---------------|
| 81 | US 59419 80 A | <input checked="" type="checkbox"/> | Apparatus and method for parallel decoding of variable-length instructions in a superscalar pipelined data processing system | 712/204 |
| 82 | US 59408 59 A | <input checked="" type="checkbox"/> | Emptying packed data state during execution of packed data instructions | 711/147 |
| 83 | US 59305 09 A | <input checked="" type="checkbox"/> | Method and apparatus for performing binary translation | 717/159 |
| 84 | US 59151 10 A | <input checked="" type="checkbox"/> | Branch misprediction recovery in a reorder buffer having a future file | 712/239 |
| 85 | US 59037 41 A | <input checked="" type="checkbox"/> | Method of allocating a fixed reorder buffer storage line for execution results regardless of a number of concurrently dispatched instructions | 712/218 |
| 86 | US 59013 02 A | <input checked="" type="checkbox"/> | Superscalar microprocessor having symmetrical, fixed issue positions each configured to execute a particular subset of instructions | 712/215 |
| 87 | US 58954 92 A | <input checked="" type="checkbox"/> | Processor associated blocking symbol controls for serializing the accessing of data resources in a computer system | 711/147 |
| 88 | US 58899 47 A | <input checked="" type="checkbox"/> | Apparatus and method for executing instructions that select a storage location for output values in response to an operation count | 709/213 |
| 89 | US 58838 24 A | <input checked="" type="checkbox"/> | Parallel adding and averaging circuit and method | 708/445 |
| 90 | US 58812 16 A | <input checked="" type="checkbox"/> | Register file backup queue | 714/15 |
| 91 | US 58782 44 A | <input checked="" type="checkbox"/> | Reorder buffer configured to allocate storage capable of storing results corresponding to a maximum number of concurrently receivable instructions regardless of a number of instructions received | 712/218 |
| 92 | US 58729 51 A | <input checked="" type="checkbox"/> | Reorder buffer having a future file for storing speculative instruction execution results | 712/218 |
| 93 | US 58705 96 A | <input checked="" type="checkbox"/> | Data processor allowing multifunctional instruction execution | 712/225 |
| 94 | US 58453 07 A | <input checked="" type="checkbox"/> | Auxiliary register file accessing technique | 711/2 |
| 95 | US 58420 17 A | <input checked="" type="checkbox"/> | Method and apparatus for forming a translation unit | 717/158 |
| 96 | US 58260 53 A | <input checked="" type="checkbox"/> | Speculative instruction queue and method therefor particularly suitable for variable byte-length instructions | 712/210 |
| 97 | US 58128 36 A | <input checked="" type="checkbox"/> | System for processing iterative tasks in data processing systems | 712/220 |
| 98 | US 58093 27 A | <input checked="" type="checkbox"/> | Eight-bit microcontroller having a risc architecture | 712/33 |
| 99 | US 58023 73 A | <input checked="" type="checkbox"/> | Method for providing a pipeline interpreter for a variable length instruction set | 717/139 |
| 100 | US 57872 41 A | <input checked="" type="checkbox"/> | Method and apparatus for locating exception correction routines | 714/2 |
| 101 | US 57782 46 A | <input checked="" type="checkbox"/> | Method and apparatus for efficient propagation of attribute bits in an instruction decode pipeline | 712/23 |
| 102 | US 57746 87 A | <input checked="" type="checkbox"/> | Central processing unit detecting and judging whether operation result executed by ALU in response to a first instruction code meets a predetermined condition | 712/211 |

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| 103 | US 57686 10 A | <input checked="" type="checkbox"/> | Lookahead register value generator and a superscalar microprocessor employing same | 712/23 |
| 104 | US 57652 16 A | <input checked="" type="checkbox"/> | Data processor with an efficient bit move capability and method therefor | 711/214 |
| 105 | US 57548 05 A | <input checked="" type="checkbox"/> | Instruction in a data processing system utilizing extension bits and method therefor | 712/200 |
| 106 | US 57457 80 A | <input checked="" type="checkbox"/> | Method and apparatus for source lookup within a central processing unit | 712/23 |
| 107 | US 57426 21 A | <input checked="" type="checkbox"/> | Method for implementing an add-compare-select butterfly operation in a data processing system and instruction therefor | 714/792 |
| 108 | US 57404 14 A | <input checked="" type="checkbox"/> | Method and apparatus for coordinating the use of physical registers in a microprocessor | 712/233 |
| 109 | US 57403 92 A | <input checked="" type="checkbox"/> | Method and apparatus for fast decoding of 00H and OFH mapped instructions | 712/210 |
| 110 | US 57271 94 A | <input checked="" type="checkbox"/> | Repeat-bit based, compact system and method for implementing zero-overhead loops | 712/241 |
| 111 | US 57064 66 A | <input checked="" type="checkbox"/> | Von Neumann system with harvard processor and instruction buffer | 711/125 |
| 112 | US 56994 60 A | <input checked="" type="checkbox"/> | Image compression coprocessor with data flow control and multiple processing units | 382/307 |
| 113 | US 56665 19 A | <input checked="" type="checkbox"/> | Method and apparatus for detecting and executing cross-domain calls in a computer system | 703/23 |
| 114 | US 56341 19 A | <input checked="" type="checkbox"/> | Computer processing unit employing a separate millicode branch history table | 712/240 |
| 115 | US 56257 84 A | <input checked="" type="checkbox"/> | Variable length instructions packed in a fixed length double instruction | 712/210 |
| 116 | US 56110 62 A | <input checked="" type="checkbox"/> | Specialized millicode instruction for string operations | 712/200 |
| 117 | US 55881 13 A | <input checked="" type="checkbox"/> | Register file backup queue | 714/15 |
| 118 | US 55749 25 A | <input checked="" type="checkbox"/> | Asynchronous pipeline having condition detection among stages in the pipeline | 712/25 |
| 119 | US 55640 57 A | <input checked="" type="checkbox"/> | Microprocessor architecture which facilitates input/output utilizing pairs of registers which the same address | 712/38 |
| 120 | US 55600 29 A | <input checked="" type="checkbox"/> | Data processing system with synchronization coprocessor for multiple threads | 712/25 |
| 121 | US 55442 44 A | <input checked="" type="checkbox"/> | Method for protecting an enciphered computer object code against cryptanalysis | 713/190 |
| 122 | US 54974 56 A | <input checked="" type="checkbox"/> | Apparatus for transferring information between an interrupt producer and an interrupt service environment | 714/29 |
| 123 | US 54871 59 A | <input checked="" type="checkbox"/> | System for processing shift, mask, and merge operations in one instruction | 712/223 |
| 124 | US 54559 55 A | <input checked="" type="checkbox"/> | Data processing system with device for arranging instructions | 712/208 |
| 125 | US 54427 04 A | <input checked="" type="checkbox"/> | Secure memory card with programmed controlled security access control | 711/163 |

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| 126 | US 54308 50 A | <input checked="" type="checkbox"/> | Data processing system with synchronization coprocessor for multiple threads | 719/314 |
| 127 | US 54210 29 A | <input checked="" type="checkbox"/> | Multiprocessor including system for pipeline processing of multi-functional instructions | 712/225 |
| 128 | US 54066 44 A | <input checked="" type="checkbox"/> | Apparatus and method for emulating a computer instruction set using a jump table in the host computer | 703/23 |
| 129 | US 53983 30 A | <input checked="" type="checkbox"/> | Register file backup queue | 714/15 |
| 130 | US 53903 07 A | <input checked="" type="checkbox"/> | Apparatus for a multi-data store or load instruction for transferring multiple contiguous storage locations in one transfer operation | 712/225 |
| 131 | US 53901 35 A | <input checked="" type="checkbox"/> | Parallel shift and add circuit and method | 708/518 |
| 132 | US 53865 80 A | <input checked="" type="checkbox"/> | Data processor | 712/32 |
| 133 | US 53633 22 A | <input checked="" type="checkbox"/> | Data processor with an integer multiplication function on a fractional multiplier | 708/620 |
| 134 | US 53554 65 A | <input checked="" type="checkbox"/> | Data storing device having a plurality of registers allotted for one address | 711/200 |
| 135 | US 53496 81 A | <input checked="" type="checkbox"/> | Bit searching circuit and data processor including the same | 712/227 |
| 136 | US 53455 69 A | <input checked="" type="checkbox"/> | Apparatus and method for resolving dependencies among a plurality of instructions within a storage device | 712/217 |
| 137 | US 53218 21 A | <input checked="" type="checkbox"/> | System for processing parameters in instructions of different format to execute the instructions using same microinstructions | 712/210 |
| 138 | US 52874 75 A | <input checked="" type="checkbox"/> | Data processing apparatus operable in extended or unextended virtual address spaces without software modification | 711/2 |
| 139 | US 52533 49 A | <input checked="" type="checkbox"/> | Decreasing processing time for type 1 dyadic instructions | 712/223 |
| 140 | US 52336 93 A | <input checked="" type="checkbox"/> | First-in first-out storage facility having bypassing loop thereof | 712/218 |
| 141 | US 51796 89 A | <input checked="" type="checkbox"/> | Dataprocessing device with instruction cache | 710/22 |
| 142 | US 50815 74 A | <input checked="" type="checkbox"/> | Branch control in a three phase pipelined signal processor | 712/234 |
| 143 | US 50776 59 A | <input checked="" type="checkbox"/> | Data processor employing the same microprograms for data having different bit lengths | 712/210 |
| 144 | US 50329 80 A | <input checked="" type="checkbox"/> | Information processing system with instruction address saving function corresponding to priority levels of interruption information | 712/228 |
| 145 | US 50017 53 A | <input checked="" type="checkbox"/> | Cryptographic system and process and its application | 380/29 |
| 146 | US 49929 38 A | <input checked="" type="checkbox"/> | Instruction control mechanism for a computing system with register renaming, map table and queues indicating available registers | 712/217 |
| 147 | US 49910 78 A | <input checked="" type="checkbox"/> | Apparatus and method for a pipelined central processing unit in a data processing system | 712/218 |
| 148 | US 49690 91 A | <input checked="" type="checkbox"/> | Apparatus for stack control employing mixed hardware registers and memory | 712/228 |

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| 149 | US 49511 93 A | <input checked="" type="checkbox"/> | Parallel computer with distributed shared memories and distributed task activating circuits | 711/206 |
| 150 | US 49473 15 A | <input checked="" type="checkbox"/> | System for controlling instrument using a levels data structure and concurrently running compiler task and operator task | 717/111 |
| 151 | US 49439 15 A | <input checked="" type="checkbox"/> | Apparatus and method for synchronization of a coprocessor unit in a pipelined central processing unit | 712/34 |
| 152 | US 48962 58 A | <input checked="" type="checkbox"/> | Data processor provided with instructions which refer to both tagged and tagless data | 712/236 |
| 153 | US 48961 33 A | <input checked="" type="checkbox"/> | Parallel string processor and method for a minicomputer | 340/146 .2 |
| 154 | US 48844 14 A | <input checked="" type="checkbox"/> | Adaptive defrost system | 62/156 |
| 155 | US 47945 17 A | <input checked="" type="checkbox"/> | Three phased pipelined signal processor | 712/32 |
| 156 | US 47775 87 A | <input checked="" type="checkbox"/> | System for processing single-cycle branch instruction in a pipeline having relative, absolute, indirect and trap addresses | 712/235 |
| 157 | US 47713 76 A | <input checked="" type="checkbox"/> | Processor | 703/27 |
| 158 | US 47681 49 A | <input checked="" type="checkbox"/> | System for managing a plurality of shared interrupt handlers in a linked-list data structure | 710/47 |
| 159 | US 47632 55 A | <input checked="" type="checkbox"/> | Method for generating short form instructions in an optimizing compiler | 717/153 |
| 160 | US 47617 31 A | <input checked="" type="checkbox"/> | Look-ahead instruction fetch control for a cache memory | 711/156 |
| 161 | US 47606 08 A | <input checked="" type="checkbox"/> | Image processing method and apparatus | 382/295 |
| 162 | US 47046 78 A | <input checked="" type="checkbox"/> | Function set for a microcomputer | 718/106 |
| 163 | US 46548 17 A | <input checked="" type="checkbox"/> | Real time controller | 712/208 |
| 164 | US 45970 44 A | <input checked="" type="checkbox"/> | Apparatus and method for providing a composite descriptor in a data processing system | 713/100 |
| 165 | US 45743 49 A | <input checked="" type="checkbox"/> | Apparatus for addressing a larger number of instruction addressable central processor registers than can be identified by a program instruction | 711/154 |
| 166 | US 45424 76 A | <input checked="" type="checkbox"/> | Arithmetic logic unit | 708/518 |
| 167 | US 45354 04 A | <input checked="" type="checkbox"/> | Method and apparatus for addressing a peripheral interface by mapping into memory address space | 710/59 |
| 168 | US 45257 76 A | <input checked="" type="checkbox"/> | Arithmetic logic unit arranged for manipulating bits | 712/221 |
| 169 | US 45063 25 A | <input checked="" type="checkbox"/> | Reflexive utilization of descriptors to reconstitute computer instructions which are Huffman-like encoded | 341/65 |
| 170 | US 44970 22 A | <input checked="" type="checkbox"/> | Method and apparatus for measurements of channel operation | 714/47 |
| 171 | US 44829 68 A | <input checked="" type="checkbox"/> | Method and apparatus for robot control | 318/568 .22 |

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|-----|---------------------|-------------------------------------|---|---------------|
| 172 | US 44596 61 A | <input checked="" type="checkbox"/> | Channel address control system for a virtual machine system | 718/100 |
| 173 | US 44545 80 A | <input checked="" type="checkbox"/> | Program call method and call instruction execution apparatus | 712/242 |
| 174 | US 44307 11 A | <input checked="" type="checkbox"/> | Central processing unit | 711/215 |
| 175 | US 44197 39 A | <input checked="" type="checkbox"/> | Decentralized generation of synchronized clock control signals having dynamically selectable periods | 713/600 |
| 176 | US 44109 56 A | <input checked="" type="checkbox"/> | Exponential operation device | 708/605 |
| 177 | US 43982 45 A | <input checked="" type="checkbox"/> | Data processing system having an instruction pipeline for processing a transfer instruction | 711/214 |
| 178 | US 43982 43 A | <input checked="" type="checkbox"/> | Data processing system having a unique instruction processor system | 712/211 |
| 179 | US 43886 85 A | <input checked="" type="checkbox"/> | Central processor with apparatus for extended virtual addressing | 711/2 |
| 180 | US 43886 82 A | <input checked="" type="checkbox"/> | Microprogrammable instruction translator | 712/211 |
| 181 | US 43785 89 A | <input checked="" type="checkbox"/> | Unidirectional looped bus microcomputer architecture | 712/2 |
| 182 | US 43707 31 A | <input checked="" type="checkbox"/> | System for entering temperature control data and displaying it with the temperature scale | 219/506 |
| 183 | US 43397 93 A | <input checked="" type="checkbox"/> | Function integrated, shared ALU processor apparatus and method | 712/32 |
| 184 | US 43375 10 A | <input checked="" type="checkbox"/> | Read control system for a control storage device | 712/211 |
| 185 | US 43143 31 A | <input checked="" type="checkbox"/> | Cache unit information replacement apparatus | 711/133 |
| 186 | US 43120 36 A | <input checked="" type="checkbox"/> | Instruction buffer apparatus of a cache unit | 711/3 |
| 187 | US 43097 56 A | <input checked="" type="checkbox"/> | Method of automatically evaluating source language logic condition sets and of compiling machine executable instructions directly therefrom | 717/155 |
| 188 | US 42989 27 A | <input checked="" type="checkbox"/> | Computer instruction prefetch circuit | 712/207 |
| 189 | US 42939 07 A | <input checked="" type="checkbox"/> | Data processing apparatus having op-code extension register | 712/208 |
| 190 | US 42814 16 A | <input checked="" type="checkbox"/> | Light source system in an optical transmission repeater | 398/178 |
| 191 | US 42453 04 A | <input checked="" type="checkbox"/> | Cache arrangement utilizing a split cycle mode of operation | 711/122 |
| 192 | US 42087 16 A | <input checked="" type="checkbox"/> | Cache arrangement for performing simultaneous read/write operations | 711/3 |
| 193 | US 41819 34 A | <input checked="" type="checkbox"/> | Microprocessor architecture with integrated interrupts and cycle steals prioritized channel | 710/40 |

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| 194 | US 41722 84 A | <input checked="" type="checkbox"/> | Priority interrupt apparatus employing a plural stage shift register having separate interrupt mechanisms coupled to the different stages thereof for segregating interrupt requests according to priority levels | 710/264 |
| 195 | US 41677 79 A | <input checked="" type="checkbox"/> | Diagnostic apparatus in a data processing system | 712/212 |
| 196 | US 41562 79 A | <input checked="" type="checkbox"/> | Microprogrammed data processing unit including a multifunction secondary control store | 712/209 |
| 197 | US 41308 69 A | <input checked="" type="checkbox"/> | Microprogram controlled system | 712/208 |
| 198 | US 41268 96 A | <input checked="" type="checkbox"/> | Microprogrammed large-scale integration (LSI) microprocessor | 712/208 |
| 199 | US 41248 91 A | <input checked="" type="checkbox"/> | Memory access system | 711/100 |
| 200 | US 41158 66 A | <input checked="" type="checkbox"/> | Data processing network for communications switching system | 379/222 |

| | L # | Hits | Search Text | DBs |
|---|-----|-------|--|--------------------|
| 1 | L1 | 59740 | (bit field tag flag cod\$3 encod\$3) near10 instruction | USPAT; US-PGPUB |
| 2 | L12 | 24001 | (register argument variable static parameter value) near10 (sav\$3 stor\$3) near20 ((stack frame region space area pointer locat\$3 position) near10 (call\$3 different separate\$3 first second subroutine above below minus plus subtract\$3 add\$3)) | USPAT; US-PGPUB |
| 3 | L13 | 399 | 1 near99 12 | USPAT; US-PGPUB |
| 4 | L14 | 11017 | (register argument variable static parameter value) near10 (sav\$3 stor\$3) near20 ((stack frame region space area pointer) near10 (call\$3 different separate\$3 second subroutine above below minus plus subtract\$3 add\$3)) | USPAT; US-PGPUB |
| 5 | L15 | 164 | 1 near99 14 | USPAT; US-PGPUB |
| 6 | L16 | 235 | 13 not 15 | USPAT; US-PGPUB |

| | Document ID | U | Title | Current OR |
|----|------------------------------|-------------------------------------|--|---------------|
| 1 | US 20040 06468 2 A1 | <input type="checkbox"/> | System and method for simultaneously executing multiple conditional execution instruction groups | 712/226 |
| 2 | US 20040 05989 5 A1 | <input checked="" type="checkbox"/> | Microprocessor circuit for portable data carriers and method for operating the circuit | 712/223 |
| 3 | US 20040 03485 8 A1 | <input checked="" type="checkbox"/> | Programming a multi-threaded processor | 718/108 |
| 4 | US 20040 01981 7 A1 | <input checked="" type="checkbox"/> | Method and apparatus for imaging device and timing generator | 713/400 |
| 5 | US 20040 01592 7 A1 | <input checked="" type="checkbox"/> | Percolating hot function store/restores to colder calling functions | 717/155 |
| 6 | US 20040 00668 7 A1 | <input checked="" type="checkbox"/> | Processor and instruction control method | 712/220 |
| 7 | US 20030 23338 6 A1 | <input checked="" type="checkbox"/> | High speed virtual machine and compiler | 718/100 |
| 8 | US 20030 21719 9 A1 | <input checked="" type="checkbox"/> | Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure | 710/1 |
| 9 | US 20030 19179 2 A1 | <input checked="" type="checkbox"/> | High speed virtual machine and compiler | 718/100 |
| 10 | US 20030 18812 8 A1 | <input checked="" type="checkbox"/> | Executing stack-based instructions within a data processing apparatus arranged to apply operations to data items stored in registers | 712/202 |
| 11 | US 20030 14235 5 A1 | <input checked="" type="checkbox"/> | Image processing method and image forming apparatus | 358/2.1 |
| 12 | US 20030 14143 4 A1 | <input checked="" type="checkbox"/> | Semiconductor integrated circuit device having a plurality of photo detectors and processing elements | 250/208 .1 |
| 13 | US 20030 14033 8 A1 | <input checked="" type="checkbox"/> | Method, apparatus and article for generation of debugging information | 717/162 |
| 14 | US 20030 12374 4 A1 | <input checked="" type="checkbox"/> | Multi-resolution image data management system and method based on tiled wavelet-like transform and sparse data coding | 382/240 |
| 15 | US 20030 05108 7 A1 | <input checked="" type="checkbox"/> | Interrupt handlers used in different modes of operations | 710/260 |
| 16 | US 20020 19445 9 A1 | <input checked="" type="checkbox"/> | Method and apparatus for saving and restoring processor register values and allocating and deallocating stack memory | 712/228 |
| 17 | US 20020 18447 2 A1 | <input checked="" type="checkbox"/> | Microcomputer | 712/33 |

| | Docum ent ID | U | Title | Current OR |
|----|------------------------------|-------------------------------------|---|---------------|
| 18 | US 20020 16198 8 A1 | <input checked="" type="checkbox"/> | Data processing circuits and interfaces | 712/221 |
| 19 | US 20020 05461 2 A1 | <input checked="" type="checkbox"/> | Integrated circuit configurations and methods for providing functions for public telephones | 370/535 |
| 20 | US 20020 03289 1 A1 | <input checked="" type="checkbox"/> | Data processing system and data processing method | 714/766 |
| 21 | US 20020 00266 5 A1 | <input checked="" type="checkbox"/> | "STACK ORIENTED DATA PROCESSING DEVICE " | 712/202 |
| 22 | US 20010 04486 6 A1 | <input checked="" type="checkbox"/> | Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure | 710/305 |
| 23 | US 20010 01007 2 A1 | <input checked="" type="checkbox"/> | Instruction translator translating non-native instructions for a processor into native instructions therefor, instruction memory with such translator, and data processing apparatus using them | 712/209 |
| 24 | US 20010 01007 1 A1 | <input checked="" type="checkbox"/> | Stack oriented data processing device | 712/11 |
| 25 | US 20010 00132 8 A1 | <input checked="" type="checkbox"/> | Link apparatus and virtual machine | 717/141 |
| 26 | US 67151 42 B1 | <input checked="" type="checkbox"/> | Execution program generation method, execution program generation apparatus, execution program execution method, and computer-readable storage medium | 717/159 |
| 27 | US 66752 97 B1 | <input checked="" type="checkbox"/> | Method and apparatus for generating and using a tamper-resistant encryption key | 713/190 |
| 28 | US 66657 93 B1 | <input checked="" type="checkbox"/> | Method and apparatus for managing access to out-of-frame Registers | 712/228 |
| 29 | US 66153 00 B1 | <input checked="" type="checkbox"/> | Fast look-up of indirect branch destination in a dynamic translation system | 710/100 |
| 30 | US 65879 10 B2 | <input checked="" type="checkbox"/> | Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure | 710/306 |
| 31 | US 65570 93 B2 | <input checked="" type="checkbox"/> | Stack oriented data processing device | 712/202 |
| 32 | US 65021 83 B2 | <input checked="" type="checkbox"/> | Stack oriented data processing device | 712/202 |
| 33 | US 64809 40 B1 | <input checked="" type="checkbox"/> | Method of controlling cache memory in multiprocessor system and the multiprocessor system based on detection of predetermined software module | 711/141 |
| 34 | US 64670 82 B1 | <input checked="" type="checkbox"/> | Methods and apparatus for simulating external linkage points and control transfers in source translation systems | 717/127 |
| 35 | US 64635 24 B1 | <input checked="" type="checkbox"/> | Superscalar processor and method for incrementally issuing store instructions | 712/221 |
| 36 | US 64346 90 B1 | <input checked="" type="checkbox"/> | Microprocessor having a DSP and a CPU and a decoder discriminating between DSP-type instructions and CUP-type instructions | 712/35 |
| 37 | US 64250 47 B1 | <input checked="" type="checkbox"/> | Process containing address decoders suited to improvements in clock speed | 711/101 |

| | Docum ent ID | U | Title | Current OR |
|----|----------------------|-------------------------------------|---|----------------|
| 38 | US 64083 85 B1 | <input checked="" type="checkbox"/> | Data processor | 712/243 |
| 39 | US 64053 11 B1 | <input checked="" type="checkbox"/> | Method for storing board revision | 713/2 |
| 40 | US 64053 02 B1 | <input checked="" type="checkbox"/> | Microcomputer | 712/35 |
| 41 | US 63381 34 B1 | <input checked="" type="checkbox"/> | Method and system in a superscalar data processing system for the efficient processing of an instruction by moving only pointers to data | 712/217 |
| 42 | US 63321 86 B1 | <input checked="" type="checkbox"/> | Vector register addressing | 711/217 |
| 43 | US 63145 04 B1 | <input checked="" type="checkbox"/> | Multi-mode memory addressing using variable-length | 711/212 |
| 44 | US 63112 63 B1 | <input checked="" type="checkbox"/> | Data processing circuits and interfaces | 712/36 |
| 45 | US 63049 63 B1 | <input checked="" type="checkbox"/> | Handling exceptions occurring during processing of vector instructions | 712/244 |
| 46 | US 62826 34 B1 | <input checked="" type="checkbox"/> | Apparatus and method for processing data having a mixed vector/scalar register file | 712/210 |
| 47 | US 62759 82 B1 | <input checked="" type="checkbox"/> | Method and device enabling a fixed program to be developed | 717/168 |
| 48 | US 62694 36 B1 | <input checked="" type="checkbox"/> | Superscalar microprocessor configured to predict return addresses from a return stack storage | 712/23 |
| 49 | US 62667 27 B1 | <input checked="" type="checkbox"/> | Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure | 710/105 |
| 50 | US 62471 13 B1 | <input checked="" type="checkbox"/> | Coprocessor opcode division by data type | 712/200 |
| 51 | US 62336 37 B1 | <input checked="" type="checkbox"/> | Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure | 710/311 |
| 52 | US 62126 30 B1 | <input checked="" type="checkbox"/> | Microprocessor for overlapping stack frame allocation with saving of subroutine data into stack area | 712/242 |
| 53 | US 62090 80 B1 | <input checked="" type="checkbox"/> | Constant reconstruction processor that supports reductions in code size and processing time | 712/212 |
| 54 | US 62081 04 B1 | <input checked="" type="checkbox"/> | Robot control unit | 318/568 .11 |
| 55 | US 62055 44 B1 | <input checked="" type="checkbox"/> | Decomposition of instructions into branch and sequential code sections | 712/230 |
| 56 | US 61890 94 B1 | <input checked="" type="checkbox"/> | Recirculating register file | 712/222 |
| 57 | US 61890 92 B1 | <input checked="" type="checkbox"/> | Pipeline processor capable of reducing branch hazards with small-scale circuit | 712/241 |
| 58 | US 61700 01 B1 | <input checked="" type="checkbox"/> | System for transferring format data from format register to memory wherein format data indicating the distribution of single or double precision data type in the register bank | 708/495 |
| 59 | US 61674 71 A | <input checked="" type="checkbox"/> | Method of and apparatus for dispatching a processing element to a program location based on channel number of received data | 710/62 |
| 60 | US 61516 73 A | <input checked="" type="checkbox"/> | Data processor | 712/243 |

| | Docum ent ID | U | Title | Current OR |
|----|---------------------|-------------------------------------|---|---------------|
| 61 | US 60887 86 A | <input checked="" type="checkbox"/> | Method and system for coupling a stack based processor to register based functional unit | 712/200 |
| 62 | US 60790 12 A | <input checked="" type="checkbox"/> | Computer that selectively forces ordered execution of store and load operations between a CPU and a shared memory | 712/216 |
| 63 | US 60759 42 A | <input checked="" type="checkbox"/> | Encoding machine-specific optimization in generic byte code by using local variables as pseudo-registers | 717/138 |
| 64 | US 60147 34 A | <input checked="" type="checkbox"/> | Superscalar microprocessor configured to predict return addresses from a return stack storage | 712/23 |
| 65 | US 60095 09 A | <input checked="" type="checkbox"/> | Method and system for the temporary designation and utilization of a plurality of physical registers as a stack | 712/202 |
| 66 | US 59997 37 A | <input checked="" type="checkbox"/> | Link time optimization via dead code elimination, code motion, code partitioning, code grouping, loop analysis with code motion, loop invariant analysis and active variable to register analysis | 717/162 |
| 67 | US 59917 85 A | <input checked="" type="checkbox"/> | Determining an extremum value and its index in an array using a dual-accumulation processor | 708/207 |
| 68 | US 59875 96 A | <input checked="" type="checkbox"/> | Register rename stack for a microprocessor | 712/217 |
| 69 | US 59874 95 A | <input checked="" type="checkbox"/> | Method and apparatus for fully restoring a program context following an interrupt | 718/108 |
| 70 | US 59830 18 A | <input checked="" type="checkbox"/> | Debug interrupt-handling microcomputer | 717/127 |
| 71 | US 59822 94 A | <input checked="" type="checkbox"/> | Paging receiver which performs data communication protocol analysis through execution of control program | 340/7.4 4 |
| 72 | US 59789 04 A | <input checked="" type="checkbox"/> | Data processor | 712/233 |
| 73 | US 59665 39 A | <input checked="" type="checkbox"/> | Link time optimization with translation to intermediate program and following optimization techniques including program analysis code motion live variable set generation order analysis, dead code elimination and load invariant analysis | 717/156 |
| 74 | US 59602 10 A | <input checked="" type="checkbox"/> | Nested-loop-specialized circuitry for repeatedly performed arithmetic operations in digital signal processor and method thereof | 712/1 |
| 75 | US 59602 03 A | <input checked="" type="checkbox"/> | Assembler device and its assembling method for use in a microcomputer or other computer system | 717/151 |
| 76 | US 59601 97 A | <input checked="" type="checkbox"/> | Compiler dispatch function for object-oriented C | 717/116 |
| 77 | US 59448 00 A | <input checked="" type="checkbox"/> | Direct memory access unit having a definable plurality of transfer channels | 710/23 |
| 78 | US 59371 88 A | <input checked="" type="checkbox"/> | Instruction creation device | 717/104 |
| 79 | US 59283 57 A | <input checked="" type="checkbox"/> | Circuitry and method for performing branching without pipeline delay | 712/235 |
| 80 | US 59283 21 A | <input checked="" type="checkbox"/> | Task and stack manager for digital video decoding | 718/1 |
| 81 | US 59241 14 A | <input checked="" type="checkbox"/> | Circular buffer with two different step sizes | 711/110 |
| 82 | US 59077 16 A | <input checked="" type="checkbox"/> | Fifo buffer capable of partially erasing data set held therein | 710/54 |

| | Docum ent ID | U | Title | Current OR |
|-----|---------------------|-------------------------------------|--|---------------|
| 83 | US 59037 49 A | <input checked="" type="checkbox"/> | Method and apparatus for implementing check instructions that allow for the reuse of memory conflict information if no memory conflict occurs | 712/226 |
| 84 | US 58812 78 A | <input checked="" type="checkbox"/> | Return address prediction system which adjusts the contents of return stack storage to enable continued prediction after a mispredicted branch | 712/242 |
| 85 | US 58812 60 A | <input checked="" type="checkbox"/> | Method and apparatus for sequencing and decoding variable length instructions with an instruction boundary marker within each instruction | 712/210 |
| 86 | US 58677 26 A | <input checked="" type="checkbox"/> | Microcomputer | 712/32 |
| 87 | US 58647 07 A | <input checked="" type="checkbox"/> | Superscalar microprocessor configured to predict return addresses from a return stack storage | 712/23 |
| 88 | US 58647 06 A | <input checked="" type="checkbox"/> | Digital signal processing apparatus and information processing system | 712/35 |
| 89 | US 58505 43 A | <input checked="" type="checkbox"/> | Microprocessor with speculative instruction pipelining storing a speculative register value within branch target buffer for use in speculatively executing instructions after a return | 712/238 |
| 90 | US 57970 25 A | <input checked="" type="checkbox"/> | Processor architecture supporting speculative, out of order execution of instructions including multiple speculative branching | 712/23 |
| 91 | US 57713 66 A | <input checked="" type="checkbox"/> | Method and system for interchanging operands during complex instruction execution in a data processing system | 712/217 |
| 92 | US 57548 11 A | <input checked="" type="checkbox"/> | Instruction dispatch queue for improved instruction cache to queue timing | 712/214 |
| 93 | US 57297 23 A | <input checked="" type="checkbox"/> | Data processing unit | 712/222 |
| 94 | US 57179 46 A | <input checked="" type="checkbox"/> | Data processor | 712/225 |
| 95 | US 57088 41 A | <input checked="" type="checkbox"/> | Processor architecture providing speculative, out of order execution of instructions | 712/23 |
| 96 | US 57064 65 A | <input checked="" type="checkbox"/> | Computers having cache memory | 711/123 |
| 97 | US 57014 49 A | <input checked="" type="checkbox"/> | Data processor | 712/239 |
| 98 | US 56873 49 A | <input checked="" type="checkbox"/> | Data processor with branch target address cache and subroutine return address cache and method of operation | 711/137 |
| 99 | US 56873 36 A | <input checked="" type="checkbox"/> | Stack push/pop tracking and pairing in a pipelined processor | 712/202 |
| 100 | US 56849 72 A | <input checked="" type="checkbox"/> | Programmable servo burst sequencer for a disk drive | 711/4 |
| 101 | US 56690 12 A | <input checked="" type="checkbox"/> | Data processor and control circuit for inserting/extracting data to/from an optional byte position of a register | 712/1 |
| 102 | US 56641 35 A | <input checked="" type="checkbox"/> | Apparatus and method for reducing delays due to branches | 712/201 |
| 103 | US 56405 83 A | <input checked="" type="checkbox"/> | Programmable servo burst decoder | 713/600 |
| 104 | US 56405 38 A | <input checked="" type="checkbox"/> | Programmable timing mark sequencer for a disk drive | 703/23 |

| | Docum ent ID | U | Title | Current OR |
|-----|---------------------|-------------------------------------|--|---------------|
| 105 | US 56153 86 A | <input checked="" type="checkbox"/> | Computer architecture for reducing delays due to branch instructions | 712/238 |
| 106 | US 56066 82 A | <input checked="" type="checkbox"/> | Data processor with branch target address cache and subroutine return address cache and method of operation | 711/204 |
| 107 | US 55817 75 A | <input checked="" type="checkbox"/> | History buffer system | 712/240 |
| 108 | US 55817 19 A | <input checked="" type="checkbox"/> | Multiple block line prediction | 712/207 |
| 109 | US 55509 94 A | <input checked="" type="checkbox"/> | Condition decision circuit for a microcomputer | 712/236 |
| 110 | US 55420 60 A | <input checked="" type="checkbox"/> | Data processor including a decoding unit for decomposing a multifunctional data transfer instruction into a plurality of control codes | 712/208 |
| 111 | US 55264 98 A | <input checked="" type="checkbox"/> | Pipeline processor, with a return address stack and two stack pointers, for storing pre-return processed addresses | 712/239 |
| 112 | US 55049 01 A | <input checked="" type="checkbox"/> | Position independent code location system | 717/144 |
| 113 | US 54993 79 A | <input checked="" type="checkbox"/> | Input/output execution apparatus for a plural-OS run system | 710/40 |
| 114 | US 54816 84 A | <input checked="" type="checkbox"/> | Emulating operating system calls in an alternate instruction set using a modified code segment descriptor | 712/212 |
| 115 | US 54715 93 A | <input checked="" type="checkbox"/> | Computer processor with an efficient means of executing many instructions simultaneously | 712/235 |
| 116 | US 54695 72 A | <input checked="" type="checkbox"/> | Post compile optimizer for linkable object code | 717/152 |
| 117 | US 54506 10 A | <input checked="" type="checkbox"/> | RISC system capable of performing calls and returns without advancing or restoring window pointers | 712/41 |
| 118 | US 54148 64 A | <input checked="" type="checkbox"/> | Method for selectively saving/restoring first registers and bypassing second registers in register units based on individual lock/unlock status thereof | 712/228 |
| 119 | US 54044 70 A | <input checked="" type="checkbox"/> | Information processing apparatus for processing instructions by out-of-order execution | 712/217 |
| 120 | US 53815 47 A | <input checked="" type="checkbox"/> | Method for dynamically linking definable program elements of an interactive data processing system | 719/331 |
| 121 | US 53597 30 A | <input checked="" type="checkbox"/> | Method of operating a data processing system having a dynamic software update facility | 717/169 |
| 122 | US 53554 59 A | <input checked="" type="checkbox"/> | Pipeline processor, with return address stack storing only pre-return processed addresses for judging validity and correction of unprocessed address | 712/242 |
| 123 | US 53455 70 A | <input checked="" type="checkbox"/> | Microprogram control circuit | 712/248 |
| 124 | US 53353 34 A | <input checked="" type="checkbox"/> | Data processing apparatus having a real memory region with a corresponding fixed memory protection key value and method for allocating memories therefor | 711/164 |
| 125 | US 53218 25 A | <input checked="" type="checkbox"/> | Processing system with lock spaces for providing critical section access | 711/163 |
| 126 | US 53218 22 A | <input checked="" type="checkbox"/> | Information processing system with addressing exception | 711/214 |
| 127 | US 53075 02 A | <input checked="" type="checkbox"/> | Data processing system having multiple register management for call and return operations | 712/41 |

| | Document ID | U | Title | Current OR |
|-----|---------------|-------------------------------------|---|------------|
| 128 | US 53012 89 A | <input checked="" type="checkbox"/> | Cache device for supplying a fixed word length of a variable instruction code and instruction fetch device | 711/213 |
| 129 | US 53012 31 A | <input checked="" type="checkbox"/> | User defined function facility | 713/191 |
| 130 | US 52972 39 A | <input checked="" type="checkbox"/> | Compile type knowledge processing tool, a high-speed inference method therefor and a system using the tool | 706/59 |
| 131 | US 52936 24 A | <input checked="" type="checkbox"/> | Data chaining mechanism for SCSI devices | 710/5 |
| 132 | US 52261 32 A | <input checked="" type="checkbox"/> | Multiple virtual addressing using/comparing translation pairs of addresses comprising a space address and an origin address (STO) while using space registers as storage devices for a data processing system | 711/209 |
| 133 | US 52147 86 A | <input checked="" type="checkbox"/> | RISC system performing calls and returns without saving or restoring window pointers and delaying saving until multi-register areas are filled | 712/41 |
| 134 | US 51932 05 A | <input checked="" type="checkbox"/> | Pipeline processor, with return address stack storing only pre-return processed address for judging validity and correction of unprocessed address | 712/239 |
| 135 | US 50484 39 A | <input checked="" type="checkbox"/> | Computerized sewing machine | 112/458 |
| 136 | US 50364 58 A | <input checked="" type="checkbox"/> | Information processor executing interruption program without saving contents of program counter | 712/244 |
| 137 | US 50310 96 A | <input checked="" type="checkbox"/> | Method and apparatus for compressing the execution time of an instruction stream executing in a pipelined processor | 711/169 |
| 138 | US 49929 32 A | <input checked="" type="checkbox"/> | Data processing device with data buffer control | 712/237 |
| 139 | US 49723 15 A | <input checked="" type="checkbox"/> | Data flow machine | 712/201 |
| 140 | US 48502 04 A | <input checked="" type="checkbox"/> | Adaptive defrost system with ambient condition change detector | 62/234 |
| 141 | US 48477 59 A | <input checked="" type="checkbox"/> | Register selection mechanism and organization of an instruction prefetch buffer | 710/53 |
| 142 | US 48071 20 A | <input checked="" type="checkbox"/> | Temporal garbage collector with indirection cells | 707/206 |
| 143 | US 48071 15 A | <input checked="" type="checkbox"/> | Instruction issuing mechanism for processors with multiple functional units | 712/215 |
| 144 | US 47991 51 A | <input checked="" type="checkbox"/> | Microprogram control circuit | 712/243 |
| 145 | US 45625 38 A | <input checked="" type="checkbox"/> | Microprocessor having decision pointer to process restore position | 714/15 |
| 146 | US 44791 94 A | <input checked="" type="checkbox"/> | System and method for reading marks on a document | 235/386 |
| 147 | US 44438 65 A | <input checked="" type="checkbox"/> | Processor module for a programmable controller | 712/242 |
| 148 | US 44124 71 A | <input checked="" type="checkbox"/> | Synchronization system for an electronic musical instrument having plural automatic play features | 84/713 |
| 149 | US 43995 07 A | <input checked="" type="checkbox"/> | Instruction address stack in the data memory of an instruction-pipelined processor | 712/219 |

| | Document ID | U | Title | Current OR |
|-----|---------------------|-------------------------------------|---|------------|
| 150 | US 43386 63 A | <input checked="" type="checkbox"/> | Calling instructions for a data processing system | 712/228 |
| 151 | US 42970 29 A | <input checked="" type="checkbox"/> | Apparatus and method for diagnostic entry | 355/133 |
| 152 | US 42413 99 A | <input checked="" type="checkbox"/> | Calling instructions for a data processing system | 712/228 |
| 153 | US 42413 97 A | <input checked="" type="checkbox"/> | Central processor unit for executing instructions with a special operand specifier of indeterminate length | 711/220 |
| 154 | US 42413 96 A | <input checked="" type="checkbox"/> | Tagged pointer handling apparatus | 711/154 |
| 155 | US 42401 42 A | <input checked="" type="checkbox"/> | Data processing apparatus providing autoincrementing of memory pointer registers | 712/42 |
| 156 | US 42362 06 A | <input checked="" type="checkbox"/> | Central processor unit for executing instructions of variable length | 712/204 |
| 157 | US 41047 21 A | <input checked="" type="checkbox"/> | Hierarchical security mechanism for dynamically assigning security levels to object programs | 711/164 |
| 158 | US 40902 37 A | <input checked="" type="checkbox"/> | Processor circuit | 711/212 |
| 159 | US 40794 55 A | <input checked="" type="checkbox"/> | Microprocessor architecture | 712/42 |
| 160 | US 40578 50 A | <input checked="" type="checkbox"/> | Processing link control device for a data processing system processing data by executing a main routine and a sub-routine | 712/242 |
| 161 | US 40286 70 A | <input checked="" type="checkbox"/> | Fetch instruction for operand address calculation | 712/209 |
| 162 | US 39846 70 A | <input checked="" type="checkbox"/> | Expandable digital arithmetic logic register stack | 708/190 |
| 163 | US 39434 94 A | <input checked="" type="checkbox"/> | Distributed execution processor | 712/226 |
| 164 | US 37542 18 A | <input checked="" type="checkbox"/> | DATA HANDLING SYSTEM WITH RELOCATION CAPABILITY COMPRISING OPERAND REGISTERS ADAPTED THEREFOR | 711/220 |

| | L # | Hits | Search Text | DBs |
|----|-----|-------|---|-------------------------------------|
| 1 | L1 | 59740 | (bit field tag flag cod\$3 encod\$3) near10 instruction | USPAT; US-PGPUB |
| 2 | L12 | 24001 | (register argument variable static parameter value) near10 (sav\$3 stor\$3) near20 ((stack frame region space area pointer locat\$3 position) near10 (call\$3 different separate\$3 first second subroutine above below minus plus subtract\$3 add\$3)) | USPAT; US-PGPUB |
| 3 | L13 | 399 | 1 near99 12 | USPAT; US-PGPUB |
| 4 | L14 | 11017 | (register argument variable static parameter value) near10 (sav\$3 stor\$3) near20 ((stack frame region space area pointer) near10 (call\$3 different separate\$3 second subroutine above below minus plus subtract\$3 add\$3)) | USPAT; US-PGPUB |
| 5 | L15 | 164 | 1 near99 14 | USPAT; US-PGPUB |
| 6 | L16 | 235 | 13 not 15 | USPAT; US-PGPUB |
| 7 | L17 | 19133 | (bit field tag flag cod\$3 encod\$3) near10 instruction | EPO; JPO; DERWENT; IBM_TDB |
| 8 | L20 | 4403 | (register argument variable static parameter value) near10 (sav\$3 stor\$3) near20 ((stack frame region space area pointer locat\$3 position) near10 (call\$3 different separate\$3 first second subroutine above below minus plus subtract\$3 add\$3 allocat\$3)) | EPO; JPO; DERWENT; IBM_TDB |
| 9 | L21 | 97 | 17 and 20 | EPO; JPO; DERWENT; IBM_TDB |
| 10 | L22 | 24825 | (register argument variable static parameter value) near10 (sav\$3 stor\$3) near20 ((stack frame region space area pointer locat\$3 position) near10 (call\$3 different separate\$3 first second subroutine above below minus plus subtract\$3 add\$3 allocat\$3)) | USPAT; US-PGPUB |
| 11 | L24 | 18 | 1 near99 22 not 13 | USPAT; US-PGPUB |
| 12 | L25 | 29280 | (register argument variable static parameter value) near10 (sav\$3 stor\$3) near20 ((stack frame region space area pointer locat\$3 position) near20 (call\$3 different separate\$3 first second subroutine above below minus plus subtract\$3 add\$3 allocat\$3)) | USPAT; US-PGPUB |
| 13 | L26 | 129 | 1 near99 25 not 13 | USPAT; US-PGPUB |
| 14 | L27 | 5372 | (register argument variable static parameter value) near10 (sav\$3 stor\$3) near20 ((stack frame region space area pointer locat\$3 position) near20 (call\$3 different separate\$3 first second subroutine above below minus plus subtract\$3 add\$3 allocat\$3)) | EPO; JPO; DERWENT; IBM_TDB |
| 15 | L28 | 20 | 17 and 27 not 21 | EPO; JPO; DERWENT; IBM_TDB |

| | Docum ent ID | U | Title | Current OR |
|----|------------------------------|-------------------------------------|---|---------------|
| 1 | US 20010 02197 1 A1 | <input type="checkbox"/> | SYSTEM FOR EXECUTING INSTRUCTIONS HAVING FLAG FOR INDICATING DIRECT OR INDIRECT SPECIFICATION OF A LENGTH OF OPERAND DATA | 712/215 |
| 2 | US 64387 45 B1 | <input checked="" type="checkbox"/> | Program conversion apparatus | 717/137 |
| 3 | US 64347 43 B1 | <input checked="" type="checkbox"/> | Method and apparatus for allocating stack slots | 717/157 |
| 4 | US 63493 79 B1 | <input checked="" type="checkbox"/> | System for executing instructions having flag for indicating direct or indirect specification of a length of operand data | 712/210 |
| 5 | US 61890 89 B1 | <input checked="" type="checkbox"/> | Apparatus and method for retiring instructions in excess of the number of accessible write ports | 712/218 |
| 6 | US 61890 87 B1 | <input checked="" type="checkbox"/> | Superscalar instruction decoder including an instruction queue | 712/208 |
| 7 | US 61263 28 A | <input checked="" type="checkbox"/> | Controlled execution of partitioned code | 717/114 |
| 8 | US 59833 42 A | <input checked="" type="checkbox"/> | Superscalar microprocessor employing a future file for storing results into multiportion registers | 712/218 |
| 9 | US 59037 40 A | <input checked="" type="checkbox"/> | Apparatus and method for retiring instructions in excess of the number of accessible write ports | 712/217 |
| 10 | US 57969 74 A | <input checked="" type="checkbox"/> | Microcode patching apparatus and method | 712/211 |
| 11 | US 57969 73 A | <input checked="" type="checkbox"/> | Method and apparatus for decoding one or more complex instructions into concurrently dispatched simple instructions | 712/208 |
| 12 | US 57297 48 A | <input checked="" type="checkbox"/> | Call template builder and method | 717/137 |
| 13 | US 55985 60 A | <input checked="" type="checkbox"/> | Tracking condition codes in translation code for different machine architectures | 717/159 |
| 14 | US 54189 58 A | <input checked="" type="checkbox"/> | Register allocation by decomposing, re-connecting and coloring hierarchical program regions | 717/156 |
| 15 | US 53392 38 A | <input checked="" type="checkbox"/> | Register usage tracking in translating code for different machine architectures by forward and reverse tracing through the program flow graph | 717/159 |
| 16 | US 53074 92 A | <input checked="" type="checkbox"/> | Mapping assembly language argument list references in translating code for different machine architectures | 717/159 |
| 17 | US 53013 25 A | <input checked="" type="checkbox"/> | Use of stack depth to identify architecture and calling standard dependencies in machine code | 717/159 |
| 18 | US 44868 31 A | <input checked="" type="checkbox"/> | Multi-programming data processing system process suspension | 718/100 |

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|----|---------------------------|-------------------------------------|---|------------|
| 1 | JP 20000 29865 A | <input type="checkbox"/> | DATA PROCESSOR | |
| 2 | JP 10312 281 A | <input checked="" type="checkbox"/> | METHOD AND SYSTEM FOR PROCESSING INSTRUCTION | |
| 3 | JP 07072 908 A | <input checked="" type="checkbox"/> | PROGRAMMABLE CONTROLLER | |
| 4 | JP 05298 099 A | <input checked="" type="checkbox"/> | CONTINUOUS PROCESSING METHOD FOR PLURAL PROGRAMS AND CENTRAL PROCESSING UNIT USING THE SAME | |
| 5 | JP 01260 537 A | <input checked="" type="checkbox"/> | EQUIPMENT CONTROL PROCESSOR CIRCUIT | |
| 6 | JP 01116 828 A | <input checked="" type="checkbox"/> | DATA ARITHMETIC PROCESSING DEVICE | |
| 7 | JP 01003 750 A | <input checked="" type="checkbox"/> | PROGRAM TRACING SYSTEM | |
| 8 | JP 63247 834 A | <input checked="" type="checkbox"/> | PROCESSING METHOD FOR PSEUDO INSTRUCTION OF FLOATING POINT FUNCTION | |
| 9 | JP 61161 545 A | <input checked="" type="checkbox"/> | DATA PROCESSING SYSTEM | |
| 10 | EP 63471 7 A2 | <input checked="" type="checkbox"/> | Data processing unit. | |
| 11 | EP 21599 2 A1 | <input checked="" type="checkbox"/> | Method for storing the control code of a processor allowing effective code modification and addressing circuit therefor. | |
| 12 | KR 20010 53729 A | <input checked="" type="checkbox"/> | Signal recording method in data service in mobile communication area | |
| 13 | US 57400 93 A | <input checked="" type="checkbox"/> | Computer with quadruple precision compatibility - includes 128-bit register file and 128-bit floating point load and store and software emulator which perform quad precision calculations on data stored in memory | |
| 14 | US 55009 48 A | <input checked="" type="checkbox"/> | Instruction pointer translation method for accessing on-chip instruction cache - by comparing upper order bit of logical address with stored values in first and second logical register | |
| 15 | US 54370 11 A | <input checked="" type="checkbox"/> | Graphics computer system - has CPUs contg. 1st ALUs including base register and offset register, and graphics hardware contg. 2nd ALUs for processing data from graphics memory circuits in parallel with 1st ALUs processing addresses of data in graphics memory circuits | |
| 16 | GB 22393 34 A | <input checked="" type="checkbox"/> | Computer system employing object-oriented memory protection - provides communication between execution environment using supervisor stack pointer and procedure entry type field | |
| 17 | US 47517 03 A | <input checked="" type="checkbox"/> | Storing control code of processor allowing effective code modification - using addressing circuit to fetch instructions which are stored in RAM instead of RAM memory | |
| 18 | EP 21599 2 A | <input checked="" type="checkbox"/> | Method for storing the control code of a processor - allowing effective code modification and addressing circuit therefor | |
| 19 | EP 17039 8 A | <input checked="" type="checkbox"/> | Data processor with program scanner - scans sequence of incoming codes and employs RAMs to detect various types of syllables in code | |
| 20 | EP 40703 A | <input checked="" type="checkbox"/> | Enhancement of 370 type data processor - reduces overhead incurred by multiple users by permitting program in one address space to obtain access to data in another address space | |

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| 1 | US 20040 06468 3 A1 | <input type="checkbox"/> | System and method for conditionally executing an instruction dependent on a previously existing condition | 712/226 |
| 2 | US 20040 03102 2 A1 | <input checked="" type="checkbox"/> | Information processing device for multiple instruction sets with reconfigurable mechanism | 717/139 |
| 3 | US 20040 01988 4 A1 | <input checked="" type="checkbox"/> | Eliminating cold register store/restores within hot function prolog/epilogs | 717/154 |
| 4 | US 20040 01570 7 A1 | <input checked="" type="checkbox"/> | Control system for protecting external program codes | 713/189 |
| 5 | US 20030 13577 9 A1 | <input checked="" type="checkbox"/> | Microprocessor | 713/600 |
| 6 | US 20030 10579 3 A1 | <input checked="" type="checkbox"/> | Long instruction word controlling plural independent processor operations | 708/625 |
| 7 | US 20030 07911 4 A1 | <input checked="" type="checkbox"/> | Processor, compiling apparatus, and compile program recorded on a recording medium | 712/213 |
| 8 | US 20010 05414 0 A1 | <input checked="" type="checkbox"/> | MICROPROCESSOR INCLUDING AN EFFICIENT IMPLEMENTATION OF EXTREME VALUE INSTRUCTIONS | 712/223 |
| 9 | US 20010 02197 1 A1 | <input type="checkbox"/> | SYSTEM FOR EXECUTING INSTRUCTIONS HAVING FLAG FOR INDICATING DIRECT OR INDIRECT SPECIFICATION OF A LENGTH OF OPERAND DATA | 712/215 |
| 10 | US 66437 75 B1 | <input checked="" type="checkbox"/> | Use of code obfuscation to inhibit generation of non-use-restricted versions of copy protected software applications | 713/190 |
| 11 | US 65570 98 B2 | <input checked="" type="checkbox"/> | Microprocessor including an efficient implementation of extreme value instructions | 712/223 |
| 12 | US 64906 73 B1 | <input checked="" type="checkbox"/> | Processor, compiling apparatus, and compile program recorded on a recording medium | 712/213 |
| 13 | US 64877 13 B1 | <input checked="" type="checkbox"/> | Software development system that presents a logical view of project components, facilitates their selection, and signals missing links prior to compilation | 717/105 |
| 14 | US 64809 59 B1 | <input checked="" type="checkbox"/> | Software system and associated methods for controlling the use of computer programs | 713/189 |
| 15 | US 64808 18 B1 | <input checked="" type="checkbox"/> | Debugging techniques in a multithreaded environment | 703/26 |
| 16 | US 64497 12 B1 | <input checked="" type="checkbox"/> | Emulating execution of smaller fixed-length branch/delay slot instructions with a sequence of larger fixed-length instructions | 712/227 |
| 17 | US 64387 45 B1 | <input checked="" type="checkbox"/> | Program conversion apparatus | 717/137 |
| 18 | US 64347 43 B1 | <input checked="" type="checkbox"/> | Method and apparatus for allocating stack slots | 717/157 |
| 19 | US 63670 05 B1 | <input checked="" type="checkbox"/> | System and method for synchronizing a register stack engine (RSE) and backing memory image with a processor's execution of instructions during a state saving context switch | 712/228 |
| 20 | US 63493 79 B1 | <input checked="" type="checkbox"/> | System for executing instructions having flag for indicating direct or indirect specification of a length of operand data | 712/210 |

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| 21 | US 63341 89 B1 | <input checked="" type="checkbox"/> | Use of pseudocode to protect software from unauthorized use | 713/200 |
| 22 | US 63145 13 B1 | <input checked="" type="checkbox"/> | Method and apparatus for transferring data between a register stack and a memory resource | 712/228 |
| 23 | US 62984 40 B1 | <input checked="" type="checkbox"/> | Method and system for providing multiple entry point code resources | 713/1 |
| 24 | US 62928 44 B1 | <input checked="" type="checkbox"/> | Media storage device with embedded data filter for dynamically processing data during read and write operations | 710/5 |
| 25 | US 62197 83 B1 | <input checked="" type="checkbox"/> | Method and apparatus for executing a flush RS instruction to synchronize a register stack with instructions executed by a processor | 712/228 |
| 26 | US 61890 89 B1 | <input checked="" type="checkbox"/> | Apparatus and method for retiring instructions in excess of the number of accessible write ports | 712/218 |
| 27 | US 61890 87 B1 | <input checked="" type="checkbox"/> | Superscalar instruction decoder including an instruction queue | 712/208 |
| 28 | US 61417 94 A | <input checked="" type="checkbox"/> | System and method for synchronizing access to shared variables in a virtual machine in a digital computer system | 717/118 |
| 29 | US 61263 28 A | <input checked="" type="checkbox"/> | Controlled execution of partitioned code | 717/114 |
| 30 | US 61157 77 A | <input checked="" type="checkbox"/> | LOADRS instruction and asynchronous context switch | 710/260 |
| 31 | US 61122 92 A | <input checked="" type="checkbox"/> | Code sequence for asynchronous backing store switch utilizing both the cover and LOADRS instructions | 712/200 |
| 32 | US 60759 37 A | <input checked="" type="checkbox"/> | Preprocessing of stored target routines for controlling emulation of incompatible instructions on a target processor and utilizing target processor feedback for controlling non-sequential incompatible instruction emulation | 703/23 |
| 33 | US 60651 14 A | <input checked="" type="checkbox"/> | Cover instruction and asynchronous backing store switch | 712/228 |
| 34 | US 60292 44 A | <input checked="" type="checkbox"/> | Microprocessor including an efficient implementation of extreme value instructions | 712/223 |
| 35 | US 60165 44 A | <input checked="" type="checkbox"/> | Apparatus and method for tracking changes in address size and for different size retranslate second instruction with an indicator from address size | 712/234 |
| 36 | US 60121 41 A | <input checked="" type="checkbox"/> | Apparatus for detecting and executing traps in a superscalar processor | 712/244 |
| 37 | US 59833 42 A | <input checked="" type="checkbox"/> | Superscalar microprocessor employing a future file for storing results into multiportion registers | 712/218 |
| 38 | US 59745 43 A | <input checked="" type="checkbox"/> | Apparatus and method for performing subroutine call and return operations | 712/240 |
| 39 | US 59745 24 A | <input checked="" type="checkbox"/> | Method and apparatus for reducing the number of rename registers in a processor supporting out-of-order execution | 712/23 |
| 40 | US 59448 11 A | <input checked="" type="checkbox"/> | Superscalar processor with parallel issue and execution device having forward map of operand and instruction dependencies | 712/23 |
| 41 | US 59075 00 A | <input checked="" type="checkbox"/> | Motion compensation adder for decoding/decompressing compressed moving pictures | 708/700 |
| 42 | US 59037 40 A | <input checked="" type="checkbox"/> | Apparatus and method for retiring instructions in excess of the number of accessible write ports | 712/217 |

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| 43 | US 58707 01 A | <input checked="" type="checkbox"/> | Control signal processing method and apparatus having natural language interfacing capabilities | 704/9 |
| 44 | US 58527 26 A | <input checked="" type="checkbox"/> | Method and apparatus for executing two types of instructions that specify registers of a shared logical register file in a stack and a non-stack referenced manner | 712/200 |
| 45 | US 58156 46 A | <input checked="" type="checkbox"/> | Decompression processor for video applications | 345/502 |
| 46 | US 58091 74 A | <input checked="" type="checkbox"/> | Decompression processor for video applications | 382/236 |
| 47 | US 58022 19 A | <input checked="" type="checkbox"/> | Methods and apparatus for table lookup transformation of digital images | 382/276 |
| 48 | US 57969 74 A | <input checked="" type="checkbox"/> | Microcode patching apparatus and method | 712/211 |
| 49 | US 57969 73 A | <input checked="" type="checkbox"/> | Method and apparatus for decoding one or more complex instructions into concurrently dispatched simple instructions | 712/208 |
| 50 | US 57645 07 A | <input checked="" type="checkbox"/> | Programmable controller with personal computerized ladder diagram | 700/18 |
| 51 | US 57400 93 A | <input checked="" type="checkbox"/> | 128-bit register file and 128-bit floating point load and store for quadruple precision compatibility | 708/513 |
| 52 | US 57297 48 A | <input checked="" type="checkbox"/> | Call template builder and method | 717/137 |
| 53 | US 57295 56 A | <input checked="" type="checkbox"/> | System decoder circuit with temporary bit storage and method of operation | 714/747 |
| 54 | US 56921 70 A | <input checked="" type="checkbox"/> | Apparatus for detecting and executing traps in a superscalar processor | 712/244 |
| 55 | US 56597 21 A | <input checked="" type="checkbox"/> | Processor structure and method for checkpointing instructions to maintain precise state | 712/228 |
| 56 | US 56574 54 A | <input checked="" type="checkbox"/> | Audio decoder circuit and method of operation | 375/242 |
| 57 | US 56088 88 A | <input checked="" type="checkbox"/> | Method and apparatus for mapping data of a 2-dimensional space from a linearly addressed memory system | 711/202 |
| 58 | US 55985 60 A | <input checked="" type="checkbox"/> | Tracking condition codes in translation code for different machine architectures | 717/159 |
| 59 | US 55984 83 A | <input checked="" type="checkbox"/> | MPEG video decompression processor | 382/232 |
| 60 | US 55967 34 A | <input checked="" type="checkbox"/> | Method and apparatus for programming embedded memories of a variety of integrated circuits using the IEEE test access port | 710/5 |
| 61 | US 55944 37 A | <input checked="" type="checkbox"/> | Circuit and method of unpacking a serial bitstream | 341/67 |
| 62 | US 55686 46 A | <input checked="" type="checkbox"/> | Multiple instruction set mapping | 712/209 |
| 63 | US 55663 03 A | <input checked="" type="checkbox"/> | Microcomputer with multiple CPU'S on a single chip with provision for testing and emulation of sub CPU's | 710/100 |
| 64 | US 55176 64 A | <input checked="" type="checkbox"/> | RISC system with instructions which include register area and displacement portions for accessing data stored in registers during processing | 712/41 |
| 65 | US 54974 59 A | <input checked="" type="checkbox"/> | System for testing instruction queue circuit and central processing unit having the system | 714/30 |

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| 66 | US 54370 43 A | <input checked="" type="checkbox"/> | Information processing apparatus having a register file used interchangeably both as scalar registers of register windows and as vector registers | 712/1 |
| 67 | US 54189 58 A | <input checked="" type="checkbox"/> | Register allocation by decomposing, re-connecting and coloring hierarchical program regions | 717/156 |
| 68 | US 54044 71 A | <input checked="" type="checkbox"/> | Method and apparatus for switching address generation modes in CPU having plural address generation modes | 712/207 |
| 69 | US 53865 66 A | <input checked="" type="checkbox"/> | Inter-processor communication method for transmitting data and processor dependent information predetermined for a receiving process of another processor | 719/310 |
| 70 | US 53793 56 A | <input checked="" type="checkbox"/> | Decompression processor for video applications | 382/233 |
| 71 | US 53392 38 A | <input checked="" type="checkbox"/> | Register usage tracking in translating code for different machine architectures by forward and reverse tracing through the program flow graph | 717/159 |
| 72 | US 53074 92 A | <input checked="" type="checkbox"/> | Mapping assembly language argument list references in translating code for different machine architectures | 717/159 |
| 73 | US 53013 25 A | <input checked="" type="checkbox"/> | Use of stack depth to identify architecture and calling standard dependencies in machine code | 717/159 |
| 74 | US 52416 79 A | <input checked="" type="checkbox"/> | Data processor for executing data saving and restoration register and data saving stack with corresponding stack storage for each register | 710/260 |
| 75 | US 52376 66 A | <input checked="" type="checkbox"/> | Apparatus using address of a predetermined preceding instruction and target instruction address stored in history table to prefetch target instruction | 712/240 |
| 76 | US 52010 56 A | <input checked="" type="checkbox"/> | RISC microprocessor architecture with multi-bit tag extended instructions for selectively attaching tag from either instruction or input data to arithmetic operation output | 712/41 |
| 77 | US 51328 98 A | <input checked="" type="checkbox"/> | System for processing data having different formats | 712/210 |
| 78 | US 50439 18 A | <input checked="" type="checkbox"/> | Multiple bus image controller structure for color page printers | 358/1.1 6 |
| 79 | US 50364 60 A | <input checked="" type="checkbox"/> | Microprocessor having miswriting preventing function | 711/103 |
| 80 | US 49758 28 A | <input checked="" type="checkbox"/> | Multi-channel data communications controller | 710/11 |
| 81 | US 49474 11 A | <input checked="" type="checkbox"/> | Programmable clock frequency divider | 377/47 |
| 82 | US 47824 43 A | <input checked="" type="checkbox"/> | Main storage control system for virtual computing function system with plural address modes in main storage access operations | 718/100 |
| 83 | US 47559 62 A | <input checked="" type="checkbox"/> | Microprocessor having multiplication circuitry implementing a modified Booth algorithm | 708/628 |
| 84 | US 47137 50 A | <input checked="" type="checkbox"/> | Microprocessor with compact mapped programmable logic array | 712/32 |
| 85 | US 46112 86 A | <input checked="" type="checkbox"/> | Cash accounting system | 705/22 |
| 86 | US RE318 64 E | <input checked="" type="checkbox"/> | Self-test feature for appliance or electronic systems operated by microprocessor | 714/36 |
| 87 | US 44919 12 A | <input checked="" type="checkbox"/> | Data processing system with improved microsubroutine facility | 712/243 |
| 88 | US 44868 31 A | <input checked="" type="checkbox"/> | Multi-programming data processing system process suspension | 718/100 |

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| 89 | US 44398 28 A | <input checked="" type="checkbox"/> | Instruction substitution mechanism in an instruction handling unit of a data processing system | 712/226 |
| 90 | US 43062 32 A | <input checked="" type="checkbox"/> | Digital joystick control interface system for video games and the like | 345/161 |
| 91 | US 42584 29 A | <input checked="" type="checkbox"/> | Multiphase clocking for MOS electronic calculator or digital processor chip | 712/32 |
| 92 | US 42233 81 A | <input checked="" type="checkbox"/> | Lookahead memory address control system | 712/207 |
| 93 | US 41808 05 A | <input checked="" type="checkbox"/> | System for displaying character and graphic information on a color video display with unique multiple memory arrangement | 345/161 |
| 94 | US 41797 36 A | <input checked="" type="checkbox"/> | Microprogrammed computer control unit capable of efficiently executing a large repertoire of instructions for a high performance data processing unit | 712/232 |
| 95 | US 41617 26 A | <input checked="" type="checkbox"/> | Digital joystick control | 341/9 |
| 96 | US 41584 32 A | <input checked="" type="checkbox"/> | Control of self-test feature for appliances or electronic equipment operated by microprocessor | 714/46 |
| 97 | US 41584 31 A | <input checked="" type="checkbox"/> | Self-test feature for appliances or electronic systems operated by microprocessor | 714/46 |
| 98 | US 41562 78 A | <input checked="" type="checkbox"/> | Multiple control store microprogrammable control unit including multiple function register control field | 712/248 |
| 99 | US 41480 14 A | <input checked="" type="checkbox"/> | System with joystick to control velocity vector of a display cursor | 345/161 |
| 100 | US 41421 80 A | <input checked="" type="checkbox"/> | Digital joystick control interface system for video games and the like | 345/161 |
| 101 | US 41258 97 A | <input checked="" type="checkbox"/> | High speed pulse interpolator | 708/102 |
| 102 | US 41248 93 A | <input checked="" type="checkbox"/> | Microword address branching bit arrangement | 712/230 |
| 103 | US 41187 73 A | <input checked="" type="checkbox"/> | Microprogram memory bank addressing system | 711/215 |
| 104 | US 41093 10 A | <input checked="" type="checkbox"/> | Variable field length addressing system having data byte interchange | 712/243 |
| 105 | US 41077 74 A | <input checked="" type="checkbox"/> | Microprogram splatter return apparatus | 712/231 |
| 106 | US 40878 57 A | <input checked="" type="checkbox"/> | ROM-initializing apparatus | 712/231 |
| 107 | US 40549 45 A | <input checked="" type="checkbox"/> | Electronic computer capable of searching a queue in response to a single instruction | 712/227 |
| 108 | US 40429 14 A | <input checked="" type="checkbox"/> | Microprogrammed control of foreign processor control functions | 710/23 |
| 109 | US 40370 90 A | <input checked="" type="checkbox"/> | Multiphase clocking for MOS | 708/130 |
| 110 | US 40329 13 A | <input checked="" type="checkbox"/> | Coding equipment providing compressed code | 341/138 |
| 111 | US 40243 86 A | <input checked="" type="checkbox"/> | Electronic calculator or digital processor chip having test mode of operation | 714/718 |

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| 112 | US 40217 81 A | <input checked="" type="checkbox"/> | Virtual ground read-only-memory for electronic calculator or digital processor | 711/211 |
| 113 | US 40216 56 A | <input checked="" type="checkbox"/> | Data input for electronic calculator or digital processor chip | 708/139 |
| 114 | US 40140 13 A | <input checked="" type="checkbox"/> | Direct drive display system for MOS integrated circuits using segment scanning | 708/160 |
| 115 | US 40140 12 A | <input checked="" type="checkbox"/> | Segment scanning method for calculator display system | 345/46 |
| 116 | US 40126 01 A | <input checked="" type="checkbox"/> | Automatic pushbutton dial assembly for a subscriber telephone | 379/357 .04 |
| 117 | US 40126 00 A | <input checked="" type="checkbox"/> | Automatic pushbutton dial system for a subscriber telephone | 379/357 .04 |
| 118 | US 40114 14 A | <input checked="" type="checkbox"/> | Automatic dial system for a subscriber telephone | 379/357 .05 |
| 119 | US 39913 06 A | <input checked="" type="checkbox"/> | Electronic calculator or digital processor chip with separately controllable digit and segment outputs | 708/168 |
| 120 | US 39913 05 A | <input checked="" type="checkbox"/> | Electronic calculator or digital processor chip with multiple code combinations of display and keyboard scan outputs | 708/168 |
| 121 | US 39899 39 A | <input checked="" type="checkbox"/> | Electronic calculator or digital processor chip with combined functions for constant, keyboard and control bit | 708/190 |
| 122 | US 39886 04 A | <input checked="" type="checkbox"/> | Electronic calculator or digital processor chip having multiple function arithmetic unit output | 708/190 |
| 123 | US 39720 23 A | <input checked="" type="checkbox"/> | I/O data transfer control system | 710/1 |
| 124 | US 39697 04 A | <input checked="" type="checkbox"/> | Word transformation apparatus for digital information processing | 712/204 |
| 125 | US 39381 04 A | <input checked="" type="checkbox"/> | System for modifying a logic controller instruction set | 711/100 |
| 126 | US 37020 07 A | <input checked="" type="checkbox"/> | TABLE DRIVEN PROGRAM | 712/234 |
| 127 | US 36514 85 A | <input checked="" type="checkbox"/> | HOLOGRAPHIC DATA PROCESSING SYSTEM | 700/90 |
| 128 | US 36482 27 A | <input checked="" type="checkbox"/> | CORRECTING SEISMIC TRACES FOR STATIC CORRECTIONS AND NORMAL MOVEOUT | 367/53 |
| 129 | US 36180 45 A | <input checked="" type="checkbox"/> | MANAGEMENT CONTROL SUBSYSTEM FOR MULTIPROGRAMMED DATA PROCESSING SYSTEM | 712/233 |